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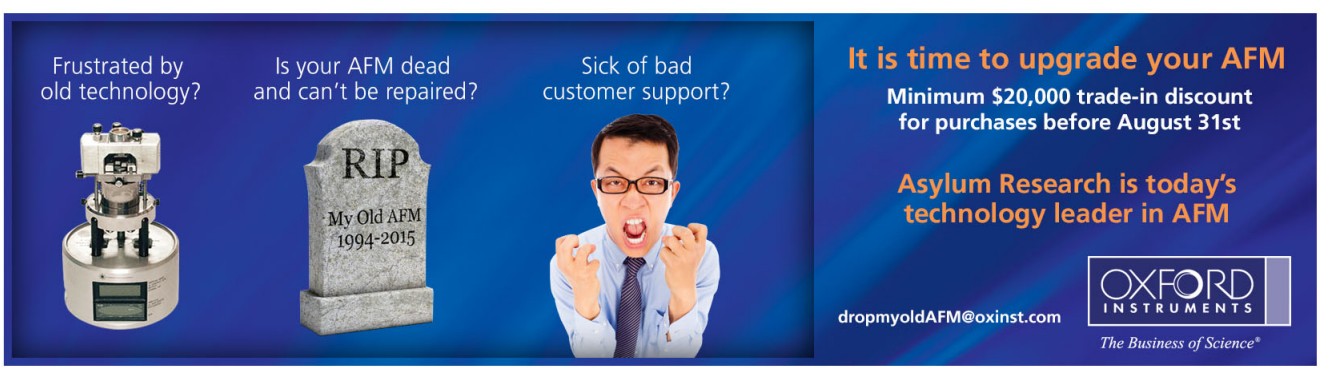

Enhanced memory effect with embedded graphene nanoplatelets in ZnO charge trapping layer

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A charge trapping memory with graphene nanoplatelets embedded in atomic layer deposited ZnO (GNIZ) is demonstrated. The memory shows a large threshold voltage V_t shift (4 V) at low operating voltage (6/−6 V), good retention (>10 yr), and good endurance characteristic ($>10^4$ cycles). This memory performance is compared to control devices with graphene nanoplatelets (or ZnO) and a thicker tunnel oxide. These structures showed a reduced V_t shift and retention characteristic. The GNIZ structure allows for scaling down the tunnel oxide thickness along with improving the memory window and retention of data. The larger V_t shift indicates that the ZnO adds available trap states and enhances the emission and retention of charges. The charge emission mechanism in the memory structures with graphene nanoplatelets at an electric field $E \geq 5.57$ MV/cm is found to be based on Fowler-Nordheim tunneling. The fabrication of this memory device is compatible with current semiconductor processing, therefore, has great potential in low-cost nano-memory applications. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4891050]

In the past decade, memory chips with low-cost, low-power consumption, and high density have gained tremendous attention due to the growing market of consumer electronic equipment such as smartphone, tablet, mobile internet devices, and digital cameras.[1,2] However, current nonvolatile flash memory devices are facing major challenges to maintain their good reliability and retention with the continuous increase in density and scaling of the gate length. Therefore, it is imperative to find novel structures and materials to be incorporated in the memory cells which would allow tunnel oxide and voltage scaling.

Recently, two-dimensional graphene and its derived nanomaterials have attracted great efforts and research due to their exceptional characteristics such as high carrier mobility, large work-function, thermal conductivity, structural robustness, and optical transparency.[3,4] Based on these unique electronic properties, graphene appears to be a promising material in nonvolatile memory devices. Graphene flash memory with large memory window and low voltage has been demonstrated, where graphene sheets were used as the floating gate of the memory.[5] However, this type of memory is less efficient and has a single point of failure because if a defect exists in the tunnel oxide, then all the stored charge in the floating gate would leak out. In this paper, we demonstrate the use of graphene nanoplatelets embedded in a ZnO layer (GNIZ) as the charge storage media in charge trapping memory devices. The performance of this device is compared to the control devices with only ZnO or graphene nanoplatelets (GN) charge storage layer with a thicker tunnel oxide in order to show the effect of GNIZ on the retention and endurance characteristics of the memory.

The MOS memory cells are fabricated on an n^+-type (111) (Antimony doped, 15–20 mΩ-cm) Si wafer. First, 3.6-nm-thick tunnel oxide Al_2O_3 followed by 2-nm-thick ZnO are deposited at 250 °C using Cambridge Nanotech Savannah-100 atomic layer deposition (ALD) system. Pristine graphene nanoplatelets (NanoIntegris PureSheets Quattro grade) are deposited by drop-casting technique. Samples are placed on hot-plate at 110 °C and 2–2.5 ml of 0.05 mg/ml graphene solution is drop-casted slowly by using plastic pipette and samples are left to dry for 5 min on hot-plate. Then a 2-nm-thick ZnO followed by a 15-nm-thick Al_2O_3 blocking oxide are ALD deposited at 250 °C. Finally, a 400-nm-thick Al layer with a diameter of 1 mm is sputtered using a shadow mask for the gate contact. A cross-sectional illustration of the fabricated memory device structure is depicted in Figure 1(a). The control structure with only GN (or only 4-nm ZnO) is fabricated the same way but with a 5-nm-thick tunnel oxide. Moreover, it should be noted that although the fabricated memory devices have 1-mm diameter, according to the ITRS roadmap the structure of such MOS memory device is expected to be scalable without degradation of performance.[1]

The charging effect in the fabricated memory cells is analyzed by studying the high frequency (1 MHz) C-V_{gate} curves of the programmed and erased states. Using the Agilent-Signatone B1505A device analyzer, the gate voltage of the memory cells is swept at −12/12 V backward and forward. The obtained memory hysteresis shows a 6.5 V, 5.5 V, and 0.9 V for the memories with GNIZ, GN, and ZnO charge trapping layer, respectively. The high frequency C-V measurement at 12/−12 V for the memory structure depicted in Figure 1 is shown in Figure 2. The significant positive shift of the V_{FB} of the erased state indicates that there is a significant amount of electrons trapped at the interfacial or in the oxide layer. In fact, the positive shift confirms the n-type nature of the ZnO layer which is due to crystallographic defects such as interstitial zinc and oxygen vacancies.[6–12] In

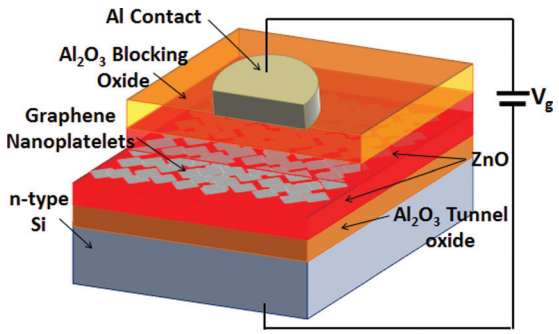

FIG. 1. Cross sectional illustration of the fabricated MOS memory with GNIZ.

addition, by sweeping the gate voltage from 12 to −12 V, the C-V curve is observed to shift positively, which indicates that the memory is being programmed by trapping electrons in the charge storage layer.

Moreover, the C-V hysteresis measurement is repeated on the three fabricated devices at different sweeping voltages. The obtained V_t shifts plotted in Figure 3 show that GNIZ memory provides the largest memory window. This is due to the thinner tunnel oxide, which exponentially increases the charge emission and tunneling probability, in addition to the additional trap states provided by the ZnO. Moreover, the figure shows that the memory with only ZnO layer does not provide a remarkable V_t shift even at high sweeping voltages (12/−12 V). This indicates that the ZnO in the GNIZ structure provides few additional trap states; however, it mainly enhances the electron retention in the graphene nanoplatelets by reducing the charge back-tunneling probability.

Since the ZnO is shown to provide only few trap states, the charge trap states density of the graphene nanoplatelets can be calculated by adopting the following equation:[11,13]

$$N_t = \frac{C_t \times \Delta V_t}{q} \quad (1)$$

where C_t is the capacitance of the memory per unit area, ΔV_t is the V_t shift, and q is the elementary charge. At 6/−6 V sweeping voltage, with a 4 V V_t shift, and C_t is 43.31 nF/cm^2, the charge trap states density is roughly 1.08×10^{12} cm^{-2}.

The virgin memory cell V_t shift is measured at room temperature and plotted vs. time as shown in Figure 4.

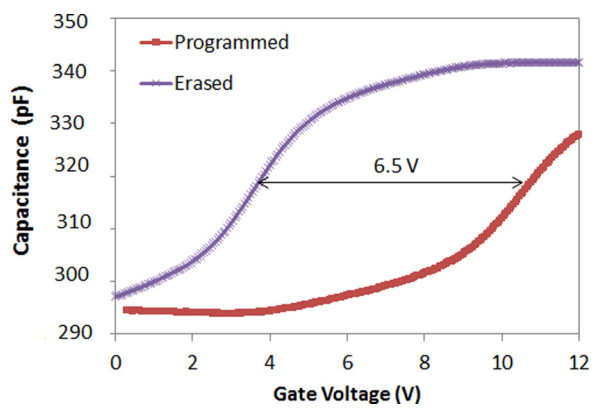

FIG. 2. C-V measurement at 12/-12 V (forward and backward) of the memory with GNIZ. The measurement is done at room temperature.

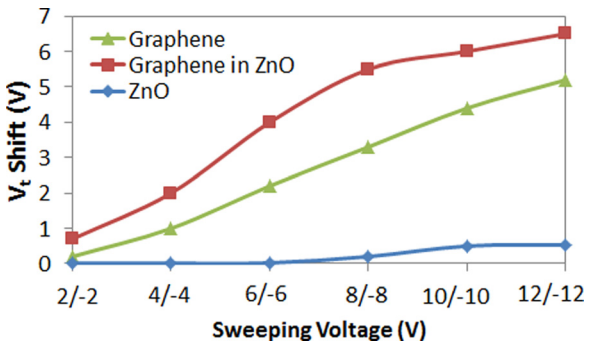

FIG. 3. Measured V_t shifts at different gate sweeping voltages for the three memory structures.

Usually, thinner tunnel oxides are associated with a degraded retention characteristic. However, the memory with GNIZ which has a 1.4 nm thinner tunnel oxide (35% thinner) showed an improved retention characteristic, where the extrapolation to 10 yr indicates a loss of 25% of the stored charge in the GNIZ memory while 29% in the GN memory. The retention measurements show that the use of ZnO in the charge storage media allows for further scaling of the tunnel oxide thickness without degrading the reliability or the retention properties of the memory.

Furthermore, the endurance characteristic of the memories with GNIZ and GN are studied. A fresh memory cell hysteresis is measured at room temperature at 10/−10 V forward and backward up to 10^4 cycles as shown in Figure 5. The V_t shift slightly reduced after 10^4 which proves the good endurance of such memory structure. In addition, the memory with GNIZ showed an improved endurance where its V_t shift reduced by 13.3%, while the memory with only GN showed a reduction of 17% after 10^4 memory hysteresis cycles.

The energy band diagram of the structure with GNIZ is depicted in Figure 6 using the reported work-function, electron affinities, and bandgap of the different materials.[7,14,15] The conduction band offset between the Si substrate and tunnel oxide is smaller than the valence band offset, which makes the electrons emission probability much higher (1.47 eV < 4.08 eV). This was proven in Figure 2, where the positive shift of the programmed state indicated electrons storage in the charge trapping layer.

Since the ZnO is observed to provide few trap states, then the majority of the electrons are expected to tunnel

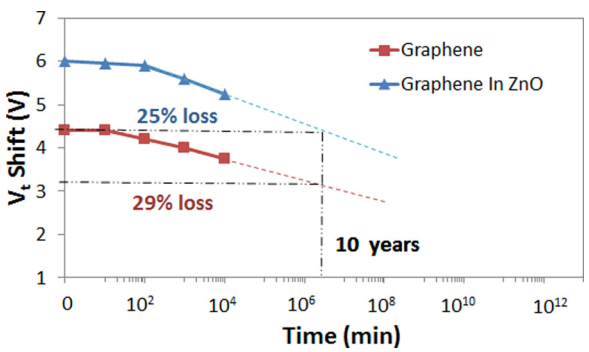

FIG. 4. V_t shift vs. time extrapolated to 10 yr with GNIZ and GN charge trapping layer.

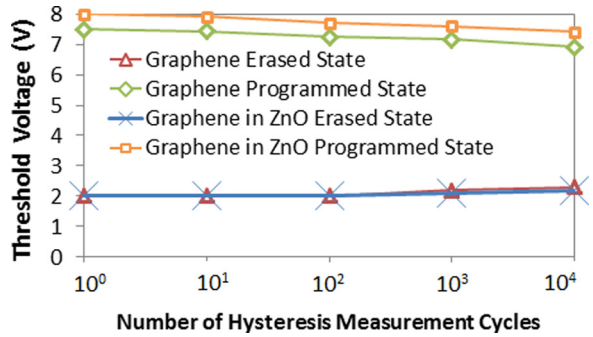

FIG. 5. Endurance measurement showing threshold voltage shift vs. number of hysteresis measurement cycles.

through the tunneling oxide to the ZnO layer and then be swept by the electric field and get trapped within the graphene nanoplatelets. Also, the additional thickness of the ZnO and the large conduction band offset between graphene and the tunnel oxide reduces the probability of back-tunneling, which improves the retention characteristic of the memory as proven in Figure 4.

The electric field across the tunnel oxide of the memory with GN is calculated using the following Gauss's law:[16]

$$\in_1 E_1 = \in_2 E_2 + Q, \tag{2}$$

$$V_g = V_1 + V_2 = d_1 E_1 + d_2 E_2, \tag{3}$$

where $\in$ is the dielectric permittivity, E is the electric field in the oxide, Q is the stored charge in the graphene nanoplatelets, V is the voltage across the oxide, d is the oxide thickness, and the subscripts 1 and 2 correspond to the tunnel and blocking oxides, respectively. The resulting electric field through the tunnel oxide is the following:

$$E_1 = \frac{V_g}{d_1 + d_2\left(\frac{\in_1}{\in_2}\right)} + \frac{Q}{\in_1 + \in_2\left(\frac{d_1}{d_2}\right)}. \tag{4}$$

The natural logarithm of the V_t shift divided by the square of the electric field is plotted vs. the reciprocal of the electric field as shown in Figure 7. The linear trend indicates that the dominant electron emission mechanism at an electric field in the tunnel oxide $E \geq 5.57$ MV/cm (corresponding to a 6 V gate voltage) is Fowler-Nordheim tunneling (F-N). In F-N tunneling, the charges are injected by tunneling into the conduction band of the oxide through a triangular energy barrier and then are swept by the electric field into the charge trapping layer. The emission rate of charges in F-N tunneling follows the equation:[16]

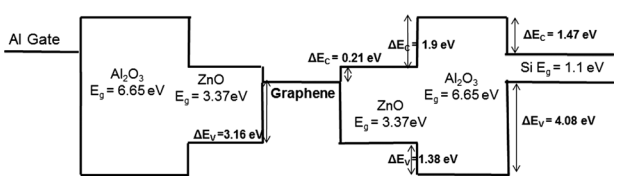

FIG. 6. Energy band diagram of the memory with GNIZ charge trapping layer. The large conduction band offset between graphene and tunnel oxide exponentially reduces the charge leakage.

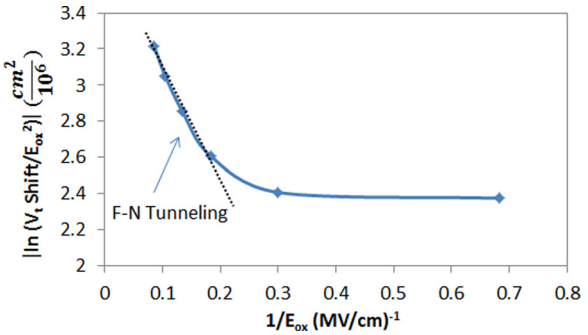

FIG. 7. Plot showing the natural logarithm of the V_t shift divided by the square of the electric field is plotted vs. the reciprocal of the electric field. The linear trend indicates that Fowler-Nordheim is the dominant emission mechanism at an oxide electric field of 5.57 MV/cm.

$$J = C_1 E_{ox}^2 e^{-\frac{C2}{E_{ox}}}, \tag{5}$$

where J is the F-N tunneling current, E_{ox} is the electric field across the tunnel oxide, and C_1 and C_2 are constants in terms of the effective mass and barrier height.

However, the addition of ZnO to the charge storage media will affect the electric field. Since the ALD ZnO is n-type, the electric field across the tunnel oxide is expected to be smaller than in the case of the GN structure. However, in the case of the GNIZ memory, the tunnel oxide thickness is 1.4 nm thinner, which would increase the electric field linearly and electron tunneling probability exponentially. Based on the larger V_t shifts obtained with GNIZ, as shown in Figure 3, the electric field and tunneling probability through the tunnel oxide are expected to be higher than that in the GN case. However, in CMOS technology,[17,18] F-N is considered as the tunneling mechanism which requires the highest electric field, therefore, F-N tunneling is expected to be the dominant electron emission mechanism in the memory with GNIZ as well. As a result, the retention of the MOS memory structure with graphene-nanoplatelets embedded in ZnO is expected to be independent of temperature since F-N tunneling is independent of temperature.[19] This have been demonstrated in Ref. 19, where the retention of fabricated Metal-Al_2O_3-Nitride-Al_2O_3-Semiconductor (MANAS) memory devices is insensitive to temperature and the main mechanism is F-N tunneling.

In conclusion, the use of graphene nanoplatelets in the charge storage media in charge trapping memory is demonstrated. With GN, the memory device showed a large V_t shift at 10/−10 V, good retention, and endurance characteristics. The use of a thinner tunnel oxide and the addition of ZnO to the charge storage media showed an improved performance of the memory, where 4 V V_t shift is achieved at 6/−6 V, with an expected loss of 25% of stored charges after 10 yr, and an endurance greater than 10^4 memory hysteresis cycle. The emission mechanism in such memory devices at electric fields higher than 5.57 MV/cm is found to be dominated by Fowler-Nordheim tunneling. Finally, this work shows that graphene nanoplatelets are a good candidate for charge trapping layers in future low-power and low-cost nonvolatile memory devices.

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